



STIC Search Report

EIC 3700

STIC Database Tracking Number: 217286

TO: Philippe Derakshani

Location: RND 10d65

Art Unit: 3754

Tuesday, March 06, 2007

Case Serial Number: 09/386505

From: Terry Solomon

Location: EIC 3700

RND 8b31

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Search Notes

No current or active litigation found involving US pat. 6380787.

Sources:

Lexis/Nexis

Questel-Orbit

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386505 (09) 6380787 April 30, 2002

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

6380787

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April 30, 2002

Integrated circuit and method for minimizing clock skews

CERT-CORRECTION: November 5, 2002 - a Certificate of Correction was issued for this patent (O.G. November 26, 2002)

APPL-NO: 386505 (09)

FILED-DATE: August 31, 1999

GRANTED-DATE: April 30, 2002

ASSIGNEE-PRE-ISSUE: August 31, 1999 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., MICRON TECHNOLOGY 8000 S. FEDERAL WAYBOISE, IDAHO, 83707, Reel and Frame Number: 010223/0096

ASSIGNEE-AT-ISSUE: Micron Technology, Inc., Boise, Idaho, United States (US), United States company or corporation (02)

LEGAL-REP: Dickstein Shapiro Morin & Oshinsky, LLP

Patent Search 6,380,787 3/6/2007

No cases found.

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** SS 1: Results 1
PRT SS 1 MAX 1 LEGALALL

1 / 1 PLUSPAT - @QUESTEL-ORBIT - image

Patent Number :

US6380787 B1 20020430 [US6380787]

Title :

(B1) Integrated circuit and method for minimizing clock skews

Patent Assignee :

(B1) MICRON TECHNOLOGY INC (US)

Patent Assignee :

Micron Technology, Inc., Boise ID [US]

Inventor(s) :

(B1) FORBES LEONARD (US)

Application Nbr :

US38650599 19990831 [1999US-0386505]

Priority Details :

US38650599 19990831 [1999US-0386505]

Intl Patent Class :

(B1) G06F-001/04 H03K-003/013

IPC Advanced All :

G06F-001/10 [2006-01 A - I R M EP]; H03K-003/356 [2006-01 A - I R M EP]

IPC Core All :

G06F-001/10 [2006 C - I R M EP]; H03K-003/00 [2006 C - I R M EP]

EPO ECLA Class :

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H03K-003/356G2

US Patent Class :

ORIGINAL (O) : 327292000; CROSS-REFERENCE (X) : 326030000 327052000
333017300

Document Type :

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US4855696; US4860322; US5086271; US5227677; US5264746; US5307381;
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US5586307; US5696953; US5811984; US5812708; US5821768; US6081162
Rabaey; "Digital Integrated Circuits" Prentice Hall Electronics and VLSI
Series.

Maliniak; "DAC attacks designer issues. (Design Automation
Conference)(includes related articles)"; 1995; 13 total pages.

Kim et al.; "Characteristics of Integrated Dipole Antennas on Bulk, SOI,
and SOS Substrates for Wireless Communications", IEEE; 1998; pp. 98-21,
98-23.

Deutsch et al.; "When are Transmission-Line Effects Important for
On-Chip Interconnections?", IEEE; 1997; pp. 1836-1845.

Publication Stage :

(B1) U.S. Patent (no pre-grant pub.) after Jan. 2, 2001

Abstract :

An integrated circuit interconnection comprising a transmission line
having a low characteristic impedance, and including a first end and a
second end. A driver is coupled to the first end of the transmission
line, and the transmission line is terminated with a current sense
amplifier having an input impedance corresponding to the characteristic
impedance of the transmission line. A plurality of components selected
from the group consisting of capacitive elements, inductive elements and
a combination of capacitive and inductive elements are connected at

spaced intervals to the transmission line between the first and second ends.
Update Code :
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1 / 1 LGST - @EPO
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20021105 US/CC-A
CERTIFICATE OF CORRECTION
Update Code :
2003-22

1 / 1 CRXX - @CLAIMS/RRX
Patent Number :
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Patent Assignee :
Micron Technology Inc
Actions :
20021126 CERTIFICATE OF CORRECTION

Session finished: 06 MAR 2007 Time 15:17:27
QUESTEL.ORBIT thanks you. Hope to hear from you again soon.